

**Notice of References Cited**

Application/Control No.

09/591,621

Applicant(s)/Patent Under

Reexamination

GUPTA, VIDYABHUSAN

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Morella I Rosales-Hanner

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**U.S. PATENT DOCUMENTS**

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-			
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	E	US-			
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**FOREIGN PATENT DOCUMENTS**

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
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	P					
	Q					
	R					
	S					
	T					

**NON-PATENT DOCUMENTS**

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Gupta, T.V.K.; Sharma, P.; Balakrishnan, M.; Malik, S.;" Processor evaluation in an embedded systems design environment", VLSI Design, 2000. Thirteenth International Conference on , 3-7 Jan. 2000, Pages:98 - 103
	V	Panda, P.R.; Dutt, N.D.; Nicolau, A.;" Local memory exploration and optimization in embedded systems", Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on , Volume: 18 , Issue: 1 , Jan. 1999, Pages:3 - 13
	W	Prete, C.A.; Graziano, M.; Lazzarini, F.;"The ChARM tool for tuning embedded systems", Micro, IEEE , Volume: 17 , Issue: 4 , July-Aug. 1997 ,Pages:67 - 76
	X	Abraham, S.G.; Mahlke, S.A.;" Automatic and efficient evaluation of memory hierarchies for embedded systems", Microarchitecture, 1999. MICRO-32. Proceedings. 32nd Annual International Symposium on , 16-18 Nov. 1999, Pages:114 - 125

\*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)

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	P					
	Q					
	R					
	S					
	T					

**NON-PATENT DOCUMENTS**

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Gries, M.; "The impact of recent DRAM architectures on embedded systems performance", Euromicro Conference, 2000. Proceedings of the 26th , Volume: 1 , 5-7 Sept. 2000, Pages:282 - 289 vol.1
	V	Kuulusa, M.; Nurmi, J.; Takala, J.; Ojala, P.; Herranen, H.; "A flexible DSP core for embedded systems", Design & Test of Computers, IEEE , Volume: 14 , Issue: 4 , Oct.-Dec. 1997, Pages:60 - 68
	W	Shackleford, B.; Yasuda, M.; Okushi, E.; Koizumi, H.; Tomiyama, H.; Yasuura, H.; "Memory-CPU Size Optimization For Embedded System Designs", Design Automation Conference, 1997. Proceedings of the 34th , June 9-13, 1997, Pages:246 - 251
	X	Danckaert, K.; Catthoor, F.; De Man, H.; "System level memory optimization for hardware-software co-design", Hardware/Software Codesign, 1997. (CODES/CASHE '97), Proceedings of the Fifth International Workshop on , 24-26 March 1997, Pages:55 - 59

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Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

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	N					
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	P					
	Q					
	R					
	S					
	T					

**NON-PATENT DOCUMENTS**

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Halambi, A.; Grun, P.; Ganesh, V.; Khare, A.; Dutt, N.; Nicolau, A.; "EXPRESSION: a language for architecture exploration through compiler/simulator retargetability", Design, Automation and Test in Europe Conference and Exhibition 1999. Proceedings ,3/1999
	V	Sudhakar, P. Rama; Kumar, Shashi; "Specification of Architecture Template for Embedded System Design", Department of Computer Science and Engineering Indian Institute of Technology, Deli; December 1999.
	W	Progress Report for "ASSET: Automated Synthesis of Embedded Systems A methodology for Heterogenous Implementations of Real Time Embedded Systems for Vision/Image Processing", Department of Computer Science and Engineering Indian Institute of Technology,
	X	Catthoor, F.; Dutt, N.D.; Kozyrakis, C.E.; "How to solve the current memory access and data transfer bottlenecks: at the processor architecture or at the compiler level?", Design, Automation and Test in Europe Conference and Exhibition 2000. Proceedings ,

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	Q					
	R					
	S					
	T					

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*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Panda, P.R.; Dutt, N.D.; Nicolau, A.; "Architectural exploration and optimization of local memory in embedded systems", System Synthesis, 1997. Proceedings., Tenth International Symposium on , 17-19 Sept. 1997, Pages:90 - 97
	V	
	W	
	X	

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